FR9839A

40V, 5A, Asynchronous Step-Down DC/DC Converter

Description

The FR9839A is an asynchronous step-down DC/DC converter that provides wide 3.5V to 40V input voltage range and 5A continuous load current capability. A wide adjustable switching frequency range allows either efficiency or external component size to be optimized. At light load condition, the FR9839A can operate at power saving mode to support high efficiency and reduce power loss.

The FR9839A fault protection includes cycle-by-cycle current limit, input UVLO, output over voltage protection and thermal shutdown. Besides, soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. Internal Compensation function reduces external compensation components and simplifies the design process. In shutdown mode, the supply current is less than 1.3μA.

The FR9839A is offered in SOP-8 (Exposed Pad) package, which provides good thermal good thermal conductance.

Features

- Wide Input Voltage Range: 3.5V to 40V
- 5A Output Current
- Adjustable Output Voltage Down to 0.75V
- 90mΩ High-Side MOSFET
- Current Mode Control
- 200kHz to 2.5MHz Adjustable Switching Frequency
- 100μA Operating Quiescent Current
- 1.3μA Shutdown Current
- Externally Adjustable Soft-Start or Internal 0.6ms Soft-Start
- Built-In Spread-Spectrum Frequency Modulation
- Input Under Voltage Lockout
- Cycle-by-Cycle Current Limit
- Hiccup Short Circuit Protection
- Output Over Voltage Protection
- Over-Temperature Protection with Auto Recovery
- SOP-8 (Exposed Pad) Package

Applications

- Industrial Power Supplies
- Automotive Battery Regulation
- Telecom and Datacom Systems
- Battery Powered System

Pin Assignments

SP Package: SOP-8 (Exposed Pad)

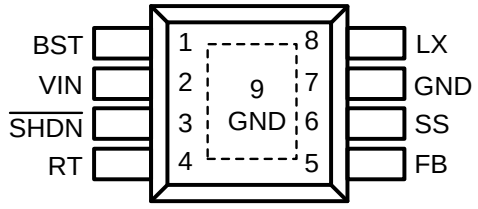


Figure 1. Pin Assignment of FR9839A

Ordering Information

FR9839A□

Package Type
SP: SOP-8 (Exposed Pad)

Typical Application Circuit

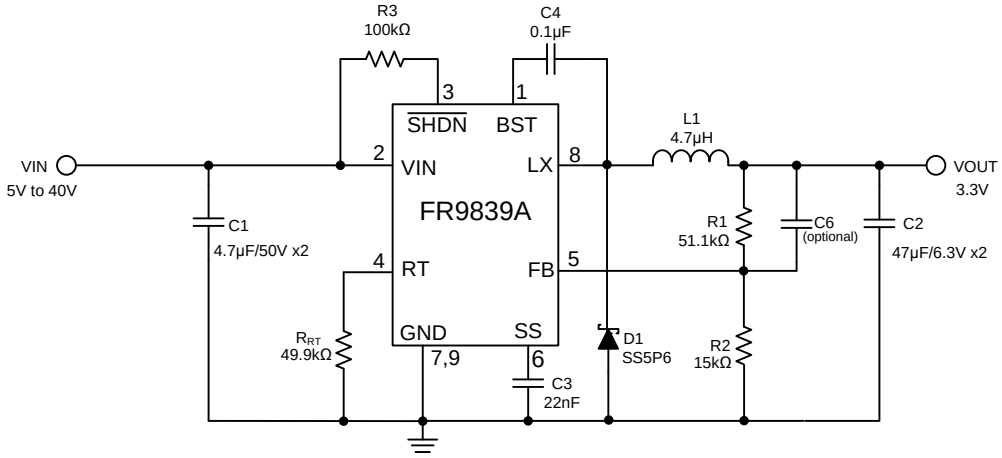


Figure 2. C_{IN} /C_{OUT} use Ceramic Capacitors Application Circuit

The recommended BOM list is as below.

V_{IN}	V_{OUT}	R1	R2	L1	C2
12V	1V	5.11kΩ	15kΩ	1.5μH	47μF MLCC x2
12V	1.2V	9.09kΩ	15kΩ	2.2μH	47μF MLCC x2
12V	1.8V	21kΩ	15kΩ	3.3μH	47μF MLCC x2
12V	2.5V	30.9kΩ	13.3kΩ	4.7μH	47μF MLCC x2
12V	3.3V	51.1kΩ	15kΩ	4.7μH	47μF MLCC x2
12V	5V	75kΩ	13.3kΩ	5.6μH	47μF MLCC x2
24V	12V	226kΩ	15kΩ	10μH	47μF MLCC x2

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No.	Pin Function
BST	**1**	High side gate drive BST pin. A capacitor rating between 100nF~1uF must be connected from this pin to LX. It can BST the gate drive to fully turn on the internal high side NMOS.
VIN	**2**	Power supply input pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
$\overline{\text{SHDN}}$	**3**	Enable input pin. This pin is a digital control input that turns the converter on or off. Connect to VIN with a 100KΩ resistor for self-startup.
RT	**4**	An internal amplifier holds this pin at a fixed voltage whwn using an external resistor to ground to set the switching frequency.
FB	**5**	Voltage feedback input pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.75V.
SS	**6**	Soft-start pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period.
GND	**7**	Ground pin. Connect GND to exposed pad.
LX	**8**	Power switching node. Connect an external inductor to this switching node.
GND (Exposed Pad)	**9**	Ground pin. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation.

Block Diagram

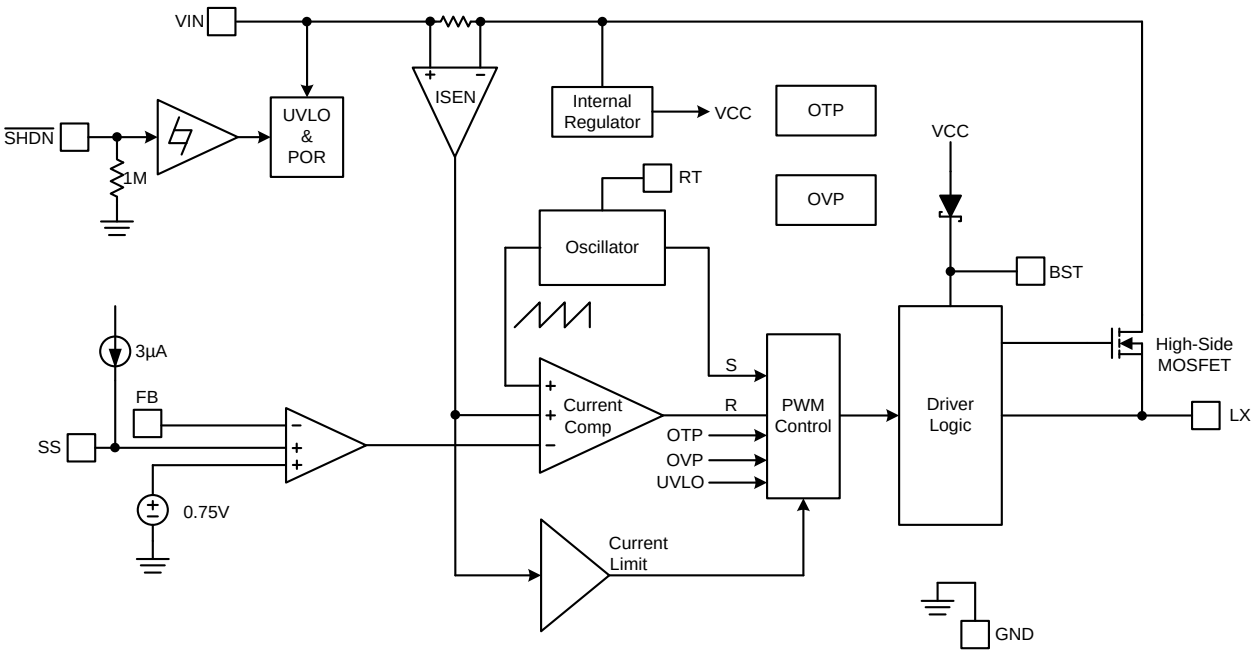


Figure 4. Block Diagram of FR9839A

Absolute Maximum Ratings (Note 1)

- Supply Voltage V_{IN} ---------- -0.3V to +44V
- BST pin Voltage V_{BST} ---------- -0.3V to V_{LX}+5V
- LX Voltage V_{LX} ---------- -3V to +44V
- Dynamic LX Voltage in 15ns Duration---------- -5V to V_{IN}+5V
- RT Pin to GND---------- -0.3V to +3.6V
- All Other Pins Voltage ---------- -0.3V to +7V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Package Thermal Resistance, (θ_{JA}) (Note 2)

  SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, (θ_{JC})

  SOP-8 (Exposed Pad) ---------- 15°C/W

Note 1: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 2: θ_{JA} is measured at 25°C ambient with the component mounted on a high effective thermal conductivity 4-layer board of JEDEC-51-7. θ_{JC} is measured at the exposed pad. The thermal resistance greatly varies with layout, copper thickness, number of layers and PCB size.

Recommended Operating Conditions

- Supply Voltage V_{IN} ---------- +3.5V to +40V
- Operating Ambient Temperature Range ---------- -40°C to +125°C
- Operating Junction Temperature Range ---------- -40°C to +150°C

Electrical Characteristics

(V_{IN}=12V, T_A= T_J = -40°C to 125°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	V_{IN}		3.5		40	V
V_{IN} Quiescent Current	I_{DDQ}	$V_{\overline{SHDN}}$=2V, V_{FB}=1V			100	μA
V_{IN} Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}$=0V		1.3	3	μA
V_{IN} Under Voltage Lockout Threshold	$V_{UVLO(Vth)}$	V_{IN} Rising		3.3		V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLO(HYS)}$			300		mV
Feedback Voltage	V_{FB}	3.5V≦V_{IN}≦40V	0.735	0.75	0.765	V
High-Side MOSFET R_{DS}(ON) (Note 3)	$R_{DS(ON)}$			90		mΩ
High-Side MOSFET Current Limit (Note 3)	$I_{LIMIT(HS)}$		6.3	7.5	8.8	A
Switching Frequency Range at RT mode	F_{LX}		200		2500	kHz
Switching Frequency	F_{LX}	R_{RT}=49.9K	450	500	550	kHz
Minimum on time (Note 3)	$T_{ON.MIN}$			75		ns
Output Under-Voltage Trip Threshold				30		%
Output Under-Voltage Trip Threshold Hysteresis				10		%
Output Under-Voltage Delay Time				24		us
V_{OUT} OVP protection				109		%
Internal Soft-Start time	T_{SS}	F_{LX} =500kHz, 0%~90% C_{SS} =NC		0.6		ms
Soft-Start Current	I_{SS}			3		μA
$\overline{SHDN}$ High-Level Input Voltage	V_{IH}		1.1			V
$\overline{SHDN}$ Low-Level Input Voltage	V_{IL}				0.4	V
Thermal Shutdown Threshold (Note 3)	T_{SD}			170		°C
Thermal Shutdown Hysteresis (Note 3)	T_{HYS}			20		°C

Note 3: Not production tested.

Function Description

The FR9839A is a high efficiency, internal compensation, and constant frequency current mode step-down Asynchronous DC/DC converter. It has integrated high-side (90mΩ, typ) power switches, and provides 5A continuous load current. It regulates input voltage from 3.5V to 40V, and down to an output voltage as low as 0.75V.

Enable

The FR9839A $\overline{SHDN}$ pin provides digital control to turn on/turn off the regulator. When the voltage of $\overline{SHDN}$ exceeds the threshold voltage, the regulator starts the soft-start function. If the $\overline{SHDN}$ pin voltage is below than the shutdown threshold voltage, the regulator will turn into the shutdown mode and the shutdown current will be smaller than 1.3μA. For auto start-up operation, connect EN to VIN through a 100kΩ resistor.

Soft-Start

The FR9839A employs adjustable soft-start function to reduce input inrush current during start up. When the device turns on, a 3μA current begins charging the C_{SS} capacitor which is connected from SS pin to GND. The C_{SS} capacitor is recommended to be maximum of 1μF. The equation for the soft start time is shown as below:

$$T_{SS}(ms)=\frac{C_{SS}(nF)\times V_{FB}}{I_{SS}(\mu A)}$$

The V_{FB} voltage is 0.75V and the I_{SS} current is 3μA. If a 0.1μF capacitor is connected from SS pin to GND, the soft start time will be 25ms.

Output Over Voltage Protection

When the FB pin voltage exceeds 109%, the output over voltage protection function will be triggered and turn off the high-side MOSFET.

Internal Compensation Function

The stability of the feedback circuit is controlled through internal compensation circuits. This internal compensation function is optimized for most applications and this function can reduce external R, C components.

Input Under Voltage Lockout

When the FR9839A is power on, the internal circuits are held inactive until V_{IN} voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 300mV (typ).

Short Circuit Protection

The FR9839A provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 0.225V, hiccup mode will be triggered to prevent the FR9839A from overheating during the extended short condition. Once the short condition is removed, the FR9839A will end the hiccup mode and return to normal.

Over Current Protection

The FR9839A over current protection function is implemented using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current also increases. When the peak inductor current reaches the current limit threshold, the output voltage starts to drop. When the over current condition is removed, the output voltage returns to the regulated value.

Over Temperature Protection

The FR9839A incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 20°C (typ).

Spread-Spectrum Operation

Due to periodicity of the switching signals, the energy concentrates in one particular frequency and also in its odds harmonics. These levels or energy is radiated and therefore this is where a potential EMI issue arises. The FR9839A have built-in spread-spectrum function and it can be enable to overcome EMI issue. The switching frequency varies by 6% relative to the switching frequency setting.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.75V. Thus the output voltage is:

$$V_{OUT}=0.75V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
5V	75kΩ	13.3kΩ
3.3V	51.1kΩ	15kΩ
2.5V	30.9kΩ	13.3kΩ
1.8V	21kΩ	15kΩ
1.2V	9.09kΩ	15kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

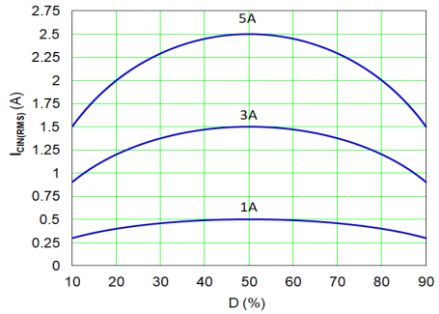
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{CIN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

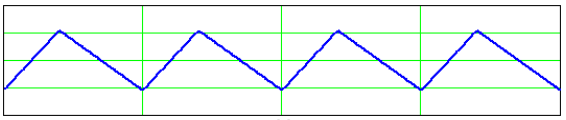
Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.

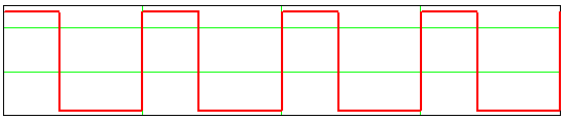
$V_{RIPPLE(ESR)}(t)$



(t)

+

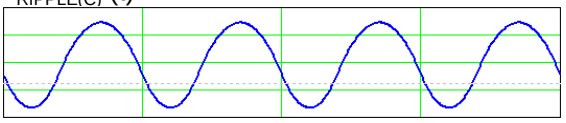
$V_{RIPPLE(ESL)}$ (t)



(t)

+

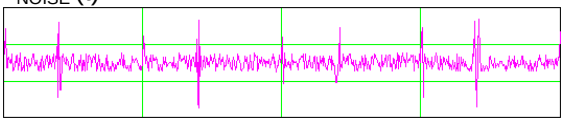
$V_{RIPPLE(C)}$ (t)



(t)

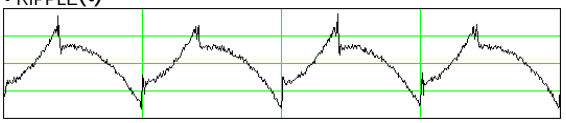
+

V_{NOISE} (t)



=

$V_{RIPPLE}(t)$



(t)

Application Information (Continued)

$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

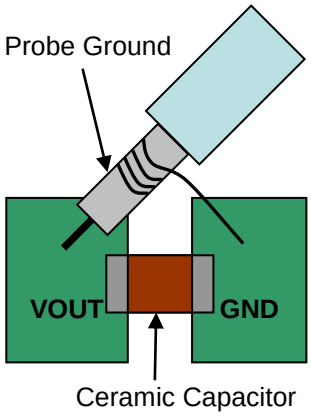
$$V_{RIPPLE(ESL)}=\frac{ESL}{L}\times V_{IN}$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC}^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirement. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminating noise.

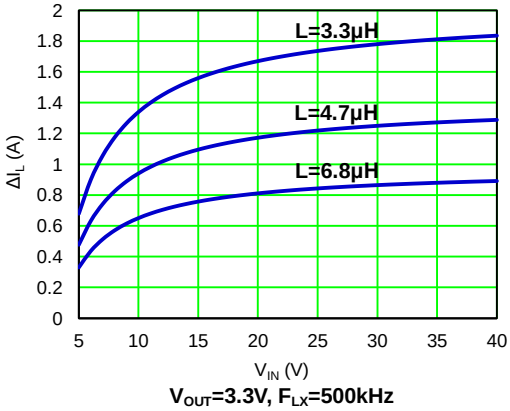


Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{LX}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphical represent ΔI_L equation.



V_{OUT}=3.3V, F_{LX}=500kHz

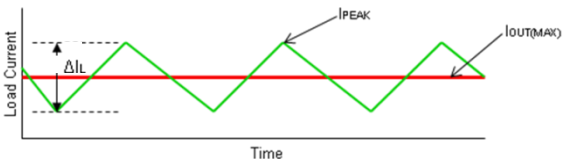
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

To guarantee sufficient output current, peak inductor current must be lower than the FR9839A high-side MOSFET current limit. The peak inductor current is as below:

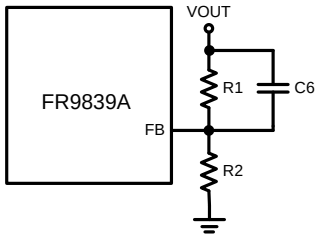
$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Feedforward Capacitor Selection

Internal compensation function allows users saving time in design and saving cost by reducing the number of external components. The use of a feedforward capacitor C6 in the feedback network is recommended to improve the transient response or higher phase margin.



For optimizing the feedforward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feedforward capacitor identified, the value of feedforward capacitor C6 can be calculated with the following equation:

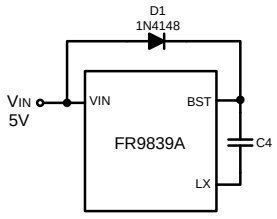
$$C6=\frac{1}{2\pi\times F_{CROSS}}\times\sqrt{\frac{1}{R1}\times\left(\frac{1}{R1}+\frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feedforward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decrease phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feedforward capacitor value can be decreased to push the cross frequency to lower region.

External Diode Selection

For 5V input applications, it is recommended to add an external BST diode. This helps improving the efficiency. The BST diode can be a low cost one such as 1N4148.



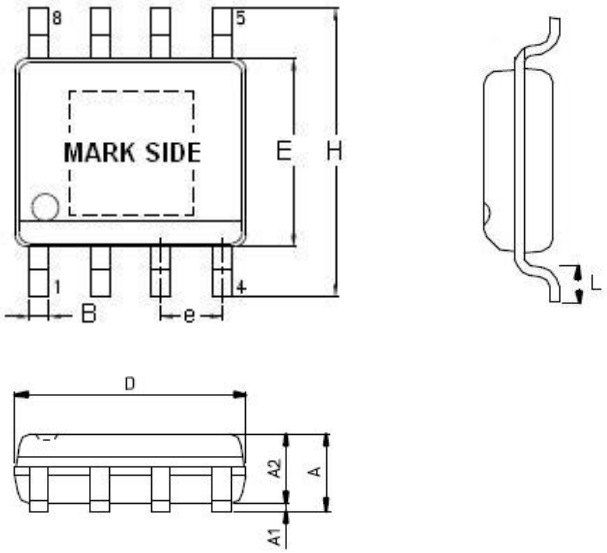
PCB Layout Recommendation

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

Outline Information

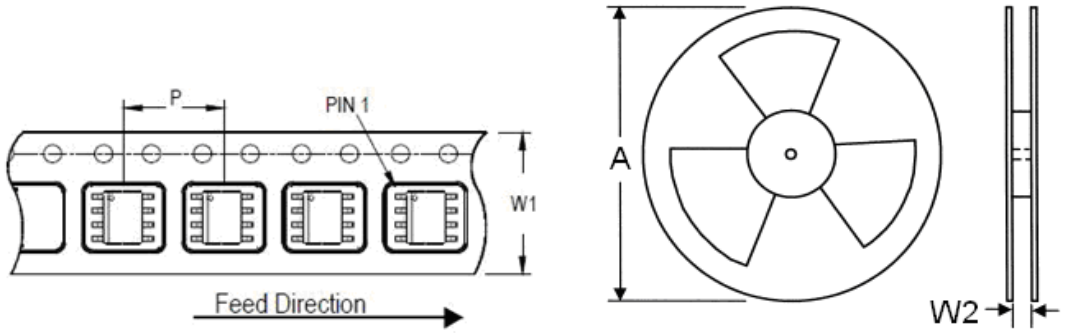
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.80
A1	0.00	0.25
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	2.80	3.50
E	3.80	4.00
E1	2.05	2.56
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note 4: Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500

Life Support Policy
Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.